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INTER-CHIP INTERFERENCE REDUCTION FOR CDMA WIRELESS COMMUNICATIONS

CROSS REFERENCE TO RELATED APPLICATION

The present invention is related to U.S. Patent Application No.

(Attorney Docket No. 01-766) entitled "DIRECT CONVERSION WIRELESS RECEIVER WITH DIGITAL PHASE EQUALIZATION" to H. Yang et al.; filed concurrently herewith and assigned to the assignee of the present invention.

BACKGROUND OF THE INVENTION

10 Field of the Invention

The present invention is related to spread spectrum wireless communications and more particularly to code division multiple access (CDMA) wireless digital transmitters and receivers.

Background Description

Third generation (3G) mobile wireless technology devices communicate using a protocol known as code division multiple access (CDMA) wherein numerous signals occupy a single transmission channel. The 3G standard known as CDMA2000 promogated by the International Telecommunications Union (ITU) supports mobile data communications at speeds ranging from 144Kbps to 2Mbps. These high 3G data rates present designers with several problems. Transmitters for 3G devices include a transmission filter that is designed, primarily to meet emission requirements. For optimum performance it is desirable that the system receivers have a filter with a transfer function response that is matched to that of the

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transmitter's filter. Any mismatch between the transmitter filter and the receiver filter impacts the receiver effectiveness by reducing receiver signal noise ratio (SNR).

A typical CDMA2000 base station transmitter signal path includes a finite impulse response (FIR) filter followed by a pre-distortion phase equalizer. The pre-distortion phase equalizer leads to a simplified mobile receiver filter which is, by contrast, a fifth order or sixth order elliptic filter. However, since the frequency response of the standard transmitter's FIR filter and predistortion equalizer cannot be matched to the frequency response of the fifth or sixth order elliptic filter, the SNR cannot be maximized for the CDMA2000 systems using current receiver designs.

Also, what is known as Inter-Chip Interference (ICI) occurs when reflected signals are delayed long enough that successive bits (or chips) in the demodulated signals overlap, creating uncertainty in the receiver data. Second generation and older systems with larger signals transmitted at a lower data rate (i.e., for voice and other low data rate applications) could tolerate this lower SNR. Unfortunately, at the higher packet speed 3G data rates and beyond (1-5 Mbps) and smaller signals that use 16 or 64 bit quadrature amplitude modulation (QAM), these same filter mismatches cause an intolerable SNR increasing ICI in the receiver, i.e., on the order of 3dB, and impact receiver performance. For backward compatibility, the same baseband filter in existing IS95/CDMA2000 systems filter high speed data packets. As a result, the current IS95/CDMA2000 based mobile baseband processor suffers from very high ICI in high speed data packets and significantly degraded system performance.

Thus, there is a need for a wireless receiver with improved signal to noise ratio that is less sensitive to inter-chip interferences.

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BRIEF DESCRIPTION OF THE INVENTION

It is a purpose of the invention to reduce wireless receiver Inter-chip Interference and improve signal to noise ratio.

The invention is a wireless communications with significantly reduced receiver inter-chip interference (ICI). The system including one or more of said transmitters with a base station baseband processor, a finite impulse response (FIR) filter, a pre-distortion phase equalizer and a digital-to-analog (DAC) converter. Receivers have an analog-to-digital (ADC) converter, a FIR filter, a phase equalizer and a receiver baseband processor. The receiver FIR filter is matched to the transmitter FIR filter and the receiver phase equalizer is matched to the pre-distortion phase equalizer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation the accompanying figures in which like references indicate similar elements and which:

Figure 1 shows a block diagram of an example of a preferred transmitter circuit for code division multiple access (CDMA) digital wireless transmission;

Figure 2 is a block diagram of an example of a preferred receiver circuit with a frequency response matched to the transmitter circuit of Figure 1;

Figure 3 shows a transfer function example for H(z) wherein FIR filters are constrained to $H_{rxeq}(z) = H_{txeq}(z^{-1})$ in the z-domain, such that $|H_{tx}(z)H_{rx}(z)|$ has linear phase and odd symmetry about half the inter-chip frequency $(f_c/2)$.

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DESCRIPTION OF PREFERRED EMBODIMENTS

Turning now to the drawings and, more particularly, Figure 1 shows a block diagram of an example of a transmitter circuit 100 for code division multiple access (CDMA) digital wireless transmission according to a preferred embodiment of the present invention. Information, e.g., voice, video or data, is encoded in a typical CDMA base station baseband processor 102. The output of the CDMA base station baseband processor 102 is passed to a finite impulse response (FIR) filter 104 with transfer function $H_{tx}(z)$. The output of the FIR filter is passed to a pre-distortion phase equalizer 106 which has a transfer function $H_{txeq}(z)$. The output of the pre-distortion phase equalizer is passed to a digital to analog converter (DAC) 108, which converts the digital signal to analog for transmission. The analog output of the DAC 108 modulates a carrier (ω_0) and, the modulated carrier is transmitted as a RF signal.

Figure 2 is a block diagram of an example of a receiver circuit 110 with a frequency response matched to the transmitter circuit 100 frequency response according to a preferred embodiment of the present invention. An RF input signal is down converted to quadrature baseband signals (i.e., real and imaginary) and each signal phase is provided to an identical parallel path, one of which is shown. Each quadrature baseband signal is passed to an analog to digital converter (ADC) 112. The output of the ADC 112 is passed to a FIR filter 114, which has a transfer response ($H_{rx}(z)$) that is matched to the transmitter FIR 104 frequency response as described hereinbelow. The output of the receiver FIR 114 is passed to a phase equalizer 116, that has a frequency response ($H_{rxeq}(z)$) that is matched to the predistortion phase equalizer 106 (in this example, they are identical) also described hereinbelow. The output of the phase equalizer 116 is passed to a mobile receiver baseband processor 118, where both quadrature signal paths converge and the transmitted information is extracted. By virtue of transmitter and receiver filters being matched, ICI is minimized in the preferred embodiment receiver.

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So, to minimize ICI, the circuit response (H(z)) for the path, from processor 102 to processor 118, must have a linear phase and flat amplitude in band and must satisfy $(H(z)=H_{tx}(z)H_{txeq}(z)H_{rx}(z)H_{rxeq}(z))$. Using this equivalent path response, H(z), the frequency response for each of the FIR filters 104, 114 and each of the phase equalizers 106, 116 may be determined. Further, by defining the transmitter FIR 104 and pre-distortion phase equalizer 106, the receiver FIR filter 114 and phase equalizer 116 are defined and vice versa. So, for example, presently a FIR filter and pre-distortion equalizer are defined by IS95/CDMA2000 for state of the art CDMA systems.

In particular, Figure 3 shows a transfer function example for H(z) wherein FIR filters 104, 114 are constrained to H_{rxeq}(z) = H_{txeq}(z⁻¹) in the z-domain, such that |H_{tx}(z)H_{rx}(z)| has linear phase and odd symmetry about the frequency fc/2, where fc is the inter-chip frequency. Since the CDMA2000 standard transmission FIR filter 104 has a transfer response (H_{tx}(z)) with on the order of 2 dB peak-to-peak ripple, to satisfy H(z), the corresponding resulting complementary receiver filter 114 must have a transfer response (H_{rx}(z)) with reverse in-band ripple. So, the combined response of the transmitter FIR filter 104 and receiver FIR filter 114 must have a flat amplitude in-band response and at least 6dB rejection at fc/2. Using a typical state of the art mathematical tool, such as Matlab from The Mathworks, Inc.,

20 multiplierless coefficients may be generated for the receiver FIR filter 114, wherein FIR filter 104 is a CDMA2000 standard transmission FIR filter.

The CDMA2000 standard defines the transmitter pre-distortion phase equalizer 106 in the S-domain. Therefore, to satisfy H(z) the receiver phase equalizer 116 must satisfy $H_{rxeq}(s)=H_{txeq}(-s)$ which transfers to the z domain as $H_{rxeq}(z)=H_{txeq}(z^{-1})$. Accordingly, the receiver phase equalizer 116 may be implemented at 2, 4 or 8 times fc, as a transfer function in z-domain, $H_{eq}(z)$, where

$$H_{eq}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}$$

and $a_0=b_2$, $a_1=b_1$ and $a_2=b_0$. Again using Matlab, multiplierless coefficients may be generated at each of the above frequencies to provide, for example:

at 4fc: a0=36, a1=-92, a2=64, and

at 8fc: a0=194, a1=-441, a2=256.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.